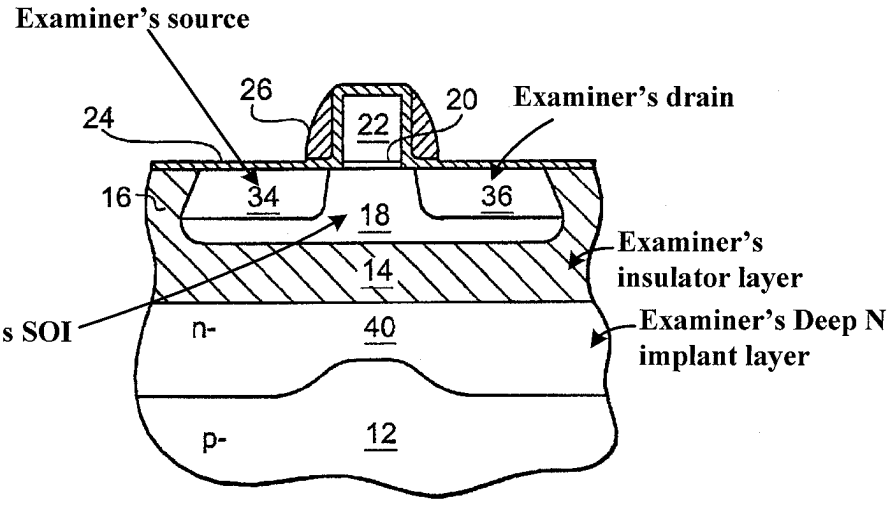
Remarks

Claims 1-3 and 12 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated October 31, 2007 listed the following objections and rejections: claims 1-3 stand rejected under 35 U.S.C. § 102(b) over Krivokapic (U.S. Patent 6,339,244); claim 12 stands rejected 35 U.S.C. § 103(a) over Krivokapic; an objection to the drawings, an objection to the specification; and claims 1-3 and 12 stand rejected under 35 U.S.C. § 112(1).

Application respectfully traverses the Section 102(b) rejection of claims 1-3 because the cited portions of the Krivokapic reference do not correspond to the claimed invention which includes, for example, aspects directed to a Deep N implant layer formed between either the source or drain and an insulator layer. The Examiner improperly asserts that Krivokapic's n-silicon region 40 is formed between buried insulator layer 14 and source/drain junctions 34 and 36. As is clearly shown in Figure 6 of the Krivokapic reference (reproduced below), buried insulator layer 14 is located between n-silicon region 40 and source/drain junctions 34 and 36.

FIG. 6



Thus, the cited portions of Krivokapic do not teach that layer 40 is formed between layer 14 and either source 34 or drain 36. Accordingly, the Section 102(b) rejection of claims 1-3 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claim 12 because the Examiner improperly asserts that claim 12 would be obvious to one of skill in the art. The

Examiner also improperly asserts that one of skill in the art would have been motivated to optimize the claimed voltage range by using routine experimentation in order to efficiently operate the device. However, further discussion regarding the impropriety of the Section 103(a) rejection of claim 12 is unnecessary at this time because the rejection fails due to the lack of correspondence between the Krivokapic reference and the claimed invention as discussed above in relation to the Section 102(b) rejection of claim 1. Accordingly, the Section 103(a) rejection of claim 12 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the objection to the drawings because the aspects of the claimed invention which the Examiner indicates form the basis for the objection are shown in Applicant's Figures. Regarding aspects of the claimed invention directed to an insulator layer between the SOI layer and the substrate layer, Applicant submits that Figure 1 shows that buried oxide layer 106 (*i.e.,* an insulator layer) is between SOI layer 104 and substrate 107. Regarding aspects of the claimed invention directed to the Deep N implant layer formed between the source and the insulator layer, Applicant submits that Figure 2 shows that Deep N layer 201 is formed between source 101 and MOS junction 105. The SOI layer 104 forms the MOS junction 105 with the buried oxide layer 106. *See, e.g.,* Paragraph 0002 of Applicant's specification. Thus, the above discussed aspects of the claimed invention are shown in the drawings and would be clear to one of skill in the art based upon Figures 1 and 2 and the related discussion in Applicant's specification. Applicant notes that drawings are only required where necessary for the understanding of the subject matter sought to be patented. *See, e.g.,* 37 CFR § 1.81 and M.P.E.P. § 608.02. Accordingly, the objection to the drawings is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the objection to the specification because there is adequate antecedent basis in the specification for aspects of the claimed invention directed to the Deep N implant layer being formed between either the source or drain and the insulator layer. For example, Applicant's Figure 2 shows that deep N layer 201 is formed between source 101 and MOS junction 105 which is formed by the intersection of SOI layer 104 and buried oxide layer 106 (*i.e.,* an insulator layer). *See, e.g.,* paragraph 0002. Thus, it would be clear to one of skill in the art based upon Applicant's

specification that deep N layer 201 is formed between source 101 and buried oxide layer 106. Accordingly, the objection to the specification is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 112(1) rejection of claims 1-3 and 12 because the claims do not contain subject matter which was not described in the specification as asserted by the Examiner. Applicant submits that support for aspects of the claimed invention directed to the Deep N implant layer being formed between either the source or drain and the insulator layer can be found, for example, in Applicant's Figures 1-2 and Paragraph 0002 of Applicant's specification. More specifically, Figure 2 shows that deep N layer 201 is formed between source 101 and MOS junction 105 which is formed by the intersection of SOI layer 104 and buried oxide layer 106 (*i.e.,* an insulator layer). Thus, the aspects of the claimed invention directed to the Deep N implant layer being formed between either the source or drain and the insulator layer are adequately disclosed in Applicant's specification. Applicant notes that word for word correspondence between the specification and the claims is not required. *See, e.g.,* M.P.E.P. § 2163. Accordingly, the Section 112(1) rejection of claims 1-3 and 12 is improper and Applicant requests that it be withdrawn.

In an effort to facilitate prosecution, Applicant has amended claim 1 to recite that the Deep N implant layer is formed between either the source or drain and the SOI layer. Applicant submits that this amendment is fully supported by Applicant's drawings and specification. *See, e.g.,* Figure 2 and Paragraphs 0010 and 0012. Applicant notes that this amendment renders the objections to the specification and drawings as well as the Section 112(1) rejection moot. Moreover, the cited portions of the Krivokapic reference do not teach that n-silicon region 40 is formed between source/drain junctions 34 and 36 and semiconductor island 18. *See, e.g.,* Figure 6 reproduced above. Accordingly, Applicant respectfully requests that this amendment be entered.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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